A New Process for Measuring and Displaying Board Test Coverage

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Board test coverage has for years been expressed as a percentage, for example, "98.2%". However it is completely unclear what this measure really means. When the product development team, test department, and manufacturing were all within one company, these groups could comfortably define what coverage meant to them. Now it is more likely these functions reside in three different companies, and each works with different sets of people and tools every day. There is little chance these groups can effectively define their own definition of coverage. Now there is a compelling reason to agree on a common definition of board test coverage.

As new board test technologies evolve [IEEE01, Park96] and probing access diminishes, test coverage becomes even more difficult to define. Worse, tester vendors have not been universally honest in their derivation of coverage, leading to overly optimistic results and invalid comparisons [TPL96]. A paper given at the 2002 International Test Conference [HPF02] proposed a metric for measuring test coverage. This metric is adopted here and expanded upon. A display GUI is then introduced to show how the metric can be viewed at high, summary levels or at low, detailed levels. Then some examples of real board coverage are given.

Background

In the past, board test coverage was loosely described as one or both of the following equations. In the first, device coverage was simply the percentage of devices that had tests, without respect to the quality of those tests. If a device type was known to be untestable on a given tester, it was often simply omitted from the total number of devices, leading to inflated claims for coverage. An example of this is when an In-Circuit test for a board does not include the parallel bypass capacitors in device coverage. It is often the case that any of these could be completely missing, and the tester would not detect it missing.

$$\text{Device Coverage} = \frac{\text{\# Devices with tests}}{\text{Total \# of devices}} \qquad \text{Shorts Coverage} = \frac{\text{\# Accessible nodes}}{\text{Total \# of nodes}}$$

In the second case of shorts testing, it was assumed (again for In-Circuit test) that if a node had a nail, it was then tested for shorts against all other nailed nodes, and that shorts coverage was simply the percentage of nodes with nails. But no accounting was made for nodes connected by small-impedance devices, such as small-valued inductors, jumpers, closed switches, etc. Yet an In-Circuit tester could not detect shorts between these nodes. Thus, for this and other reasons, test coverage claims have always been suspect.

A recent paper [HPF02] has introduced a rigorous definition of board test coverage. It starts by defining what it is we are testing for: "A *defect* is an unacceptable deviation from a norm." Defects require some sort of action, whether it be to discard a unit, or repair it, or to use the information about the defect to fix a process. We don't want to deliver defects to customers if possible. So, test coverage must be a measure of how many potential defects are detectable by a test. Note the word "detectable" is not a measure of the capability of the tester, but a measure of

the quality of the test. Most tests fall short of the full capability of a tester, for practical reasons usually driven by schedule.

Next, defects are categorized into two broad groups. The first group consists of component property defects. Component properties of interest to the board test community are:

1. Presence (the device is present)
2. Correctness (it is the correct device)
3. Orientation (if polarized, it is not reversed or rotated by 90 degrees)
4. Live (the device is basically alive – note this is not a full functional qualification)
5. Alignment (the device is centered, free of skews or small rotations).

These properties are called "PCOLA" component properties (the acronym formed from the first letter of each). Notice that the first four properties are *fundamental* to the operation of a device, whereas the last (alignment) may not affect device performance and is called a *qualitative* property. Fundamental properties are often measured by In-Circuit or functional tests, but qualitative properties usually cannot be so tested. For example, a surface-mount resistor flipped on its side (called a "billboard") may still be soldered and electrically functional, but a visual inspection would fail the board until the alignment problem was fixed. PCOLA properties define five related defects, not Present, not Correct, not Oriented correctly, not Live and improperly Aligned. The model insists that all these properties, for *all* components, must be tested in order to claim excellent coverage, with the exception of irrelevant properties such as the orientation of a non-polarized device such as a resistor.

The other broad group deals with connection properties. A connection is a place where a component is electrically attached to a board, typically a solder or press-fit joint. A resistor has two connections, an IC may have many hundreds, and components like bar code labels may have none. Connections have three interesting properties:

1. Shorts (unwanted continuity to other *nearby* connection points)
2. Opens (lack of continuity between the board and device connection)
3. Quality (free of malformation, excess or inadequate solder, cold solder voids, etc.).

Again, this yields an acronym – SOQ. Again, the first two are fundamental properties and the last is qualitative. The first two could be found with In-Circuit or functional tests, but the last typically is better tested with visual or X-ray technologies. Note the word "nearby" in the definition of shorts. Shorts are assumed *not* to exist on boards themselves between pairs of arbitrary nodes, but rather, between connections. This is consistent with manufacturing practice of doing bare-board test before mounting expensive components. Shorts are virtually always related to connections in close proximity. A given connection is a candidate for shorting to another connection if it lies within a *shorting radius*, which is defined as the maximum distance that can be bridged by connection defects. A given connection can be open or connected, but it can be potentially shorted to several other connections if the circuit is dense. Note also that connections belonging to separate devices may also be shorted, and not just connections among a single device's connections. See Figure 1.

The coverage measurement process has two major steps. The first is to enumerate a list of possible defects in terms of PCOLA and SOQ, for *all* components of a board and each of their connections. This requires *only* a bill of materials (the component list) and layout information (X-Y data). It does *not* require a netlist (which pins are connected by wires). In fact, one error of the past was to use netlist information to reduce the set of defects. For example, if two device pins were both connected to ground, then a short between them (a defect) was not counted. This may

have seemed reasonable to In-Circuit test engineers, but not to X-ray engineers. (After all, a process that creates shorts needs to be monitored in all cases, for process reliability.) This enumeration of all defects is called the *defect universe*. Once we know this defect universe, we can judge the coverage of a test by how completely it can detect the members of the defect universe. Again, a relatively complete test program will cover a larger fraction of the defect universe than a poorly constructed test program, but we do not expect any one tester to approach full coverage by itself.

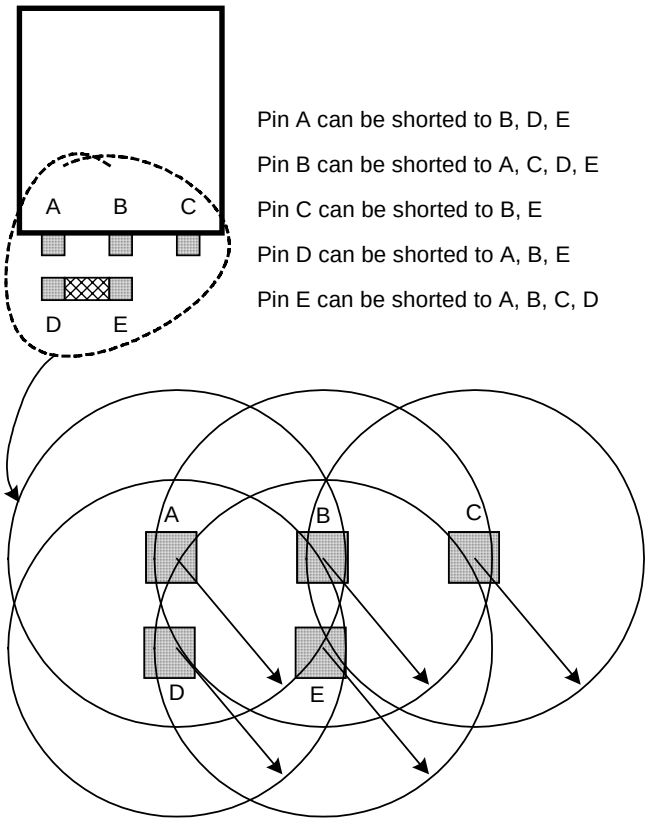


Figure 1: Shorts are unwanted connectivity between connection points within a shorting radius.

The second major step for determining coverage is to "grade" each test unit of a test program. (Test programs may be made up of hundreds or even thousands of test units. For example, a single resistor measurement is one test unit within many needed to test an entire board.) If a board is tested by more than one tester (e.g., In-Circuit, Automated Inspection and X-ray) then the contributions of each test program are accumulated. Test units are graded by asking the question "What does it mean with this test unit passes?" While it may seem reasonable to ask the opposite (what does it mean when this test unit fails?), that question can be clouded by diagnostic accuracy issues and interactions between devices, such as seen when disabling or guarding surrounding devices. Consider grading a simple passing resistor test unit on an In-Circuit tester for PCOLA/SOQ:

Presence:	if the resistor is not present, it will fail with certainty.
Correct:	if the resistor is not correct, the test *could* still pass if the value measured is right, but the resistor is the wrong type (thin film versus wirewound) or wrong wattage. We are only partially sure about correctness.
Orientation:	this is a don't care, so we don't consider it for a grade.
Live:	if the resistor test passes, it must be basically functional (not open or shorted inside).
Alignment:	nothing has been determined about this by measuring the resistor's value.
Shorts:	the two terminals of the resistor (if proximal) cannot be shorted.
Opens:	the two terminals of the resistor must be free of opens.
Quality:	we can say nothing about the quality of the solder joints.

The data in Table 1 summarize the test coverage of an In-Circuit resistor test, and also the result of Visual and X-ray tests for the same resistor. It is important to realize that with this rigorous definition of the defect universe, no single tester technology will be able to give full coverage. Clearly, inspection technologies (Visual, X-ray) have the edge on qualitative measurements (Alignment, Quality) while In-Circuit or functional will have distinct advantages for certain fundamental properties (Correct, Live). Thus, a board that you might have judged to

have 98.5% test coverage in the past may have less than 60% of the defect universe covered by this more rigorous and "test-blind" measure. By test-blind, it is meant that *no foreknowledge* of what tester is going to be used is utilized in selecting the defect universe.

	Presence	Correct	Orientation	Live	Alignment	Shorts	Open	Quality
In-Circuit	Full	Partial	NA	Full	None	Full	Full	None
Visual	Full	Full	NA	None	Full	Full	Full	Partial
X-ray	Full	None	NA	None	Full	Full	Full	Full

Table 1: Test coverage for resistor properties for In-Circuit, visual and X-ray tests.

The ITC paper [HPF02] goes on to propose a weighting scheme for component properties and connection properties, as well as for major device types. This allows a user to place more importance on certain defects and less on others. For example, you might rate Presence to be more important than Alignment and give it a higher weight. Similarly, you might want to weight Digital ICs more than termination resistors. The weighting scheme normalizes scoring such that a maximum score can be achieved by getting "Full" coverage on all non-zero-weighted device and connection properties. This maximum score is independent of board size or complexity. This allows for meaningful comparisons of board test coverage, when weighted similarly. Once you have test score data, you can then ask and answer questions such as, "Where should I spend my next hour of test development time to improve my test coverage the most?", or "Where am I at the most risk of a defect being shipped?", or "Should I improve an existing test on one tester, or add new tests on a second, different tester?".

Coverage Display

The ITC paper [HPF02] proposes using a hierarchical display for coverage data as shown in Figure 2. At the top level (the "management summary") we see two numbers given which are the device and connection total scores. We use a maximum score of 100,000 points, so a perfectly covered board would score (100,000 – 100,000).

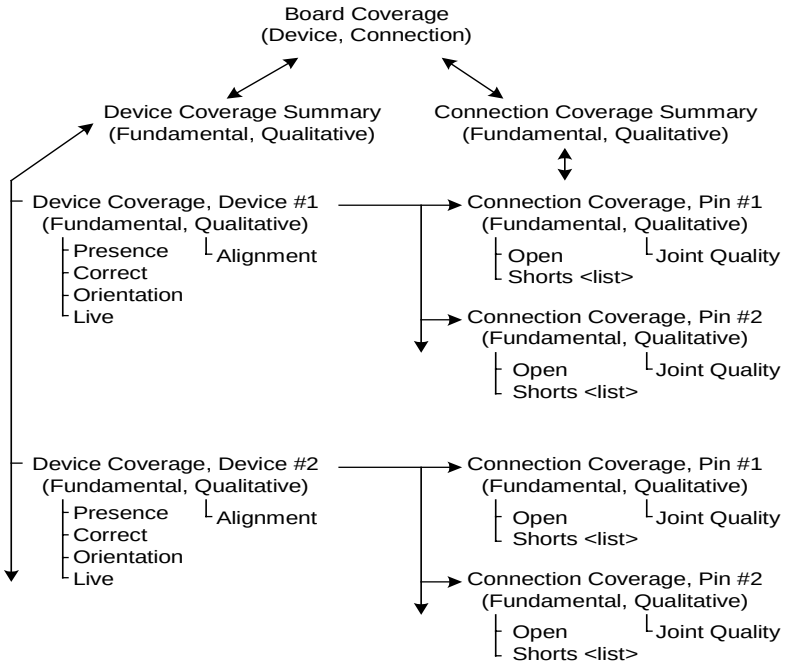
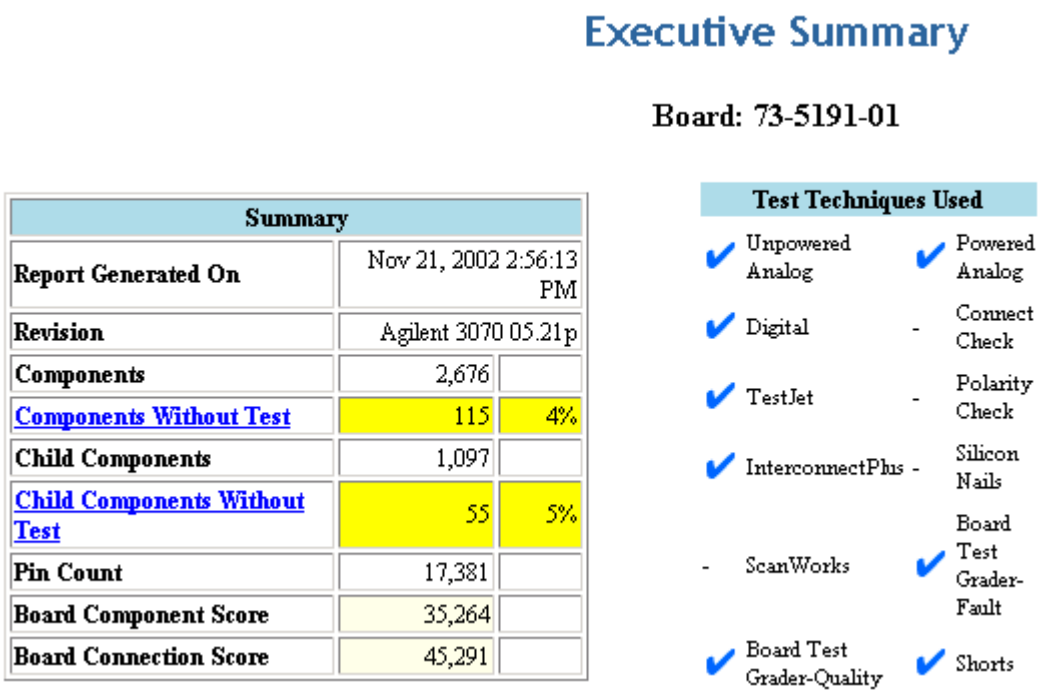


Figure 2: Device and connection coverages summarized and detailed.

Below the management summary we see each number broken down into the next level, for fundamental and qualitative property coverage. Below that we get into details on a per-device and per-connection level. This is where test engineers might spend time analyzing where they have or don't have decent coverage. There they can see the PCOLA and SOQ scores for all devices and their connections. These can be linked together for easier navigation.

Software to perform this analysis has been created, and some examples for a real board are shown here. This software monitors a board test ATE system while it is generating board tests units, to provide grading for each, and also generates the defect universe. It integrates this into a series of HTML files that contain hot links that link them together logically. For example, an HTML file for coverage of a device (e.g., digital device u79) will contain links for each pin's node. Clicking on a node sends you to an HTML file that describes the details of that node, including all the device pins it is attached to, which are themselves, hot links to each device. This allows one to easily "browse" the board structure, which for larger boards is very helpful. Otherwise you would have to page through scores of large schematic pictures.

Figure 3 shows an executive summary for an In-Circuit tested board with 2,676 devices and 17,381 connections. The board component score seems pretty low at 35,264 out of a possible 100,000. The connection score is somewhat better at 45,291 out of 100,000. Let's dig a bit deeper to see what is going on.



Executive Summary

Board: 73-5191-01

Summary		
Report Generated On	Nov 21, 2002 2:56:13 PM	
Revision	Agilent 3070 05.21p	
Components	2,676	
Components Without Test	115	4%
Child Components	1,097	
Child Components Without Test	55	5%
Pin Count	17,381	
Board Component Score	35,264	
Board Connection Score	45,291	

Test Techniques Used			
✔	Unpowered Analog	✔	Powered Analog
✔	Digital	-	Connect Check
✔	TestJet	-	Polarity Check
✔	InterconnectPlus	-	Silicon Nails
-	ScanWorks	✔	Board Test Grader-Fault
✔	Board Test Grader-Quality	✔	Shorts

Figure 3: Executive summary for a real board as displayed by an HTML browser.

In Figure 4 we see a portion of the device summary page. On the right side we see the weights used for component and connection properties. Since this is an In-Circuit (only) test, we can not get any scoring for Alignment or solder Quality. These are generally worth 0.1 and 0.2 each. So a perfect In-Circuit test score would be 90,000 – 80,000, which makes are score of 35,264 – 45291 seem more reasonable in the ICT context. Next, as you browse down a bit you come across the device type of "Capacitors – bypass". There are 1125 of these, with a component score of 0% and a connection score of 28%. This category of component scores very low on an ICT since they essentially are 1125 capacitors in parallel across the power and ground planes of the board. If one were missing, the test for the parallel combination of these would not be able to

detect this. Thus we get very poor (zero) coverage for *all* these devices, and they account for 42% of all devices on this board. You might wonder how we could have 0% device coverage, but 28% connection coverage. This occurs because we *do* get coverage of any shorts that could occur across a capacitor's pins. Many of these capacitors are very small SMT devices that have pins within the shorting radius (here, 0.1 inch).

Details				Coverage Score		Components Without Tests		Component Weights					Connection Weights		
Device Type	Components	Child Components	Unique Part No.	Component Score	Connection Score	Components	Child Components	P	C	O	L	A	S	O	Q
Analog Libraries	5	0	5	70%	52%	0%	-	0.3	0.2	0.2	0.2	0.1	0.4	0.4	0.2
Digital Libraries	82	0	36	51%	48%	21%	-	0.3	0.2	0.2	0.2	0.1	0.4	0.4	0.2
Mixed Libraries	0	0	0	-	-	-	-	0.3	0.2	0.2	0.2	0.1	0.4	0.4	0.2
Other Libraries	48	0	1	0%	21%	100%	-	0.3	0.2	0.2	0.2	0.1	0.4	0.4	0.2
Part Libraries	188	0	18	80%	70%	0%	-	0.3	0.2	0.2	0.2	0.1	0.4	0.4	0.2
Capacitors	207	0	1	50%	64%	1%	-	0.3	0.2	0.2	0.2	0.1	0.4	0.4	0.2
Capacitors - bypass	1125	0	1	0%	28%	1%	-	0.3	0.2	0.2	0.2	0.1	0.4	0.4	0.2
Resistors	949	206	1	65%	66%	0%	3%	0.35	0.25	0.0	0.25	0.15	0.4	0.4	0.2

Figure 4: Portion of device coverage summary. Underlined fields are links to detail pages.

Next consider "Digital Devices". Here we have a component score of 51% and a connection score of 48%. It turns out that 17 of the 99 digital devices have no tests at all, for whatever reason. A portion of the data appears in Figure 5.

Component Details - Digital Libraries				Coverage Scores	
Ref. Designator	Part No.	Pins	Tests	Component	Connection
u1	15-2093-01	48	'testjet' **!'u1'**	30%	65%
u2	15-2239-01	52	'testjet' **!'u2'**	30%	43%
u3	15-2922-01	28	'testjet' 'u3'	80%	70%
u4	08-0368-01	388	'u16_u77_ps' 'u58_connect' 'u56_connect' 'u77_connect' 'u6_connect' 'u4_connect' 'u68_connect' 'u74_connect' 'u72_connect' 'u57_connect' 'testjet' 'u44_connect' 'u4' 'u41_connect' 'u35_connect' 'u5_connect' 'u76_connect' 'u16_u77' 'u75_connect' 'u67_connect' 'u73_connect' 'u16_u77_bus' **!'u16_connect'**	80%	58%
			'u16_u77_ps' 'u58_connect' 'u56_connect' 'u77_connect'		

Figure 5: A portion of the coverage data for "digital devices".

Let's dig a bit deeper on a particular device, like u2. When we click on the link for u2, we find the data in Figure 6. There we find that u2 has only device coverage for Presence. It also has 52 total pins and 16 power and ground pins. We have no opens coverage on power/ground pins since they are highly redundant. This is the reason for many of the uncovered defects in digital device connections. Again, in past times, these defects were ignored, inflating the coverage

claims. Looking back at Figure 5, for u3, we see that the coverage is actually quite good, approaching the best we can do for In-Circuit test (which cannot score for qualitative defects, Alignment and solder Quality). Again, the power/ground pins account for the not-quite-perfect connection score.

Report for Reference Designator "u2"

Summary	
Part Number	15-2239-01
Device Type	Digital Libraries
Test Jet Score	62%
Board Grader Score	87%
Number of Tests	2
Number of Pins	52

Connection Coverage Scores

Digital Libraries Component Weights										Digital Libraries Connection Weights					
Presence	0.3	**Correct**	0.2	**Orientation**	0.2	**Live**	0.2	**Alignment**	0.1	**Shorts**	0.4	**Opens**	0.4	**Quality**	0.2

"u2" Component Scores					
Presence	**Correct**	**Orientation**	**Live**	**Alignment**	**Total**
Full	None	None	None	None	0.3

"u2" Connection Scores			
Shorts	**Opens**	**Quality**	**Total**
0.673	0.413	0	0.435

Pin Details			Connection Scores			
Pin Name	**Node**	**Pin Type**	**Shorts**	**Opens**	**Quality**	**Total**
1	GND_PLL	power_pin	Full	None	None	0.4
2	PM_PLL_RST_L	input	Full	Full	None	0.8
3	CKN_8	input	Partial	None	None	0.2
4	CKN_8	input	Partial	None	None	0.2
5	CKN_7	input	Full	None	None	0.4
6	PM_DCOK	input	Full	Partial	None	0.6
7	CKN_5	input	Full	Full	None	0.8
8	CKN_8	input	Partial	None	None	0.2
9	CKN_8	input	Partial	None	None	0.2
10	CKN_8	input	Partial	None	None	0.2
11	CLK62M5_1P	input	Partial	Full	None	0.6
12	CLK62M5_1N	input	Partial	Full	None	0.6
13	3V3_PLL	power_pin	Full	None	None	0.4
14	CKN_8	input	Full	None	None	0.4
15	GND	power_pin	Partial	None	None	0.2
16	CKN_62M5_BANK2	output	Partial	Full	None	0.6

Figure 6: A portion of the coverage data for digital device “u2”.

This board actually has fairly good scores as obtainable with only an In-Circuit test. We note that the coverage of bypass capacitors and redundant power/ground pins are the principle cause of coverage loss. If we were to add an X-ray test step to augment this coverage, our final coverage results would be significantly enhanced. The judgement to do this depends on the risk one perceives with having untested bypasses and potential open power/ground pins. In some products, these may be acceptable risks. In others, they may be of deep concern and an incentive to use additional testing equipment.

References

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